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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,545	09/22/2003	Timothy Chen	135432 (GECZ 2 00680)	9930

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EXAMINER	
TRAN, THUY V	
ART UNIT	**PAPER NUMBER**
2821	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,545	CHEN ET AL.	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the Applicants' filing on 09/22/2003. In virtue of this filing, claims 1-20 are currently presented in the instant application.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09/22/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings Objections

3. The drawings are objected to because of the following informalities:

- Figs. 1-5: drawing lines are not legible, not uniform; reference numerals/characters are not legible; and
- Figs. 2-3: connection nodes are not properly shown; for a proper characterization, they should be darkened.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections/ Minor Informalities

4. Claim 11 is objected to because of the following informalities:

Line 3, --;-- should be inserted after "voltage" (second occurrence);

Line 4, --;-- should be inserted after "voltage"; and

Line 6, "," after "and" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-9, 11-13, and 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Stack (U.S. Patent No. 6,222,322).

With respect to claim 1, Stack discloses, in Fig. 4, a lamp inverter starting circuit comprising (1) a switching portion [110] that converts a bus voltage signal (that goes through T3, D7; see Fig. 4) into an alternating current signal (via inverter [Q1, Q2]; see Fig. 4), (2) an input portion [106] that receives the bus voltage signal, (3) a resonant load portion [T5, C9] for receiving a lamp load [FL1], and (4) a voltage controlled start-up portion [108] that delays triggering (via diac [D9]; see col. 6, lines 45-67; and col. 7, lines 1-7) of the inverter starting circuit based on a detected voltage (which is of the diac [D9]; see col. 6, lines 56-65).

With respect to claim 2, Fig. 4 of Stack shows that the switching portion [110] includes first and second power transistors [Q1, Q2].

With respect to claim 3, Fig. 4 of Stack shows that the transistors [Q1, Q2] are field effect transistors.

With respect to claim 4, Stack further discloses, in Fig. 4, an input AC line voltage source ranging from 120 V to 230 V (which is within the claimed range of 120-280 V).

With respect to claim 6, Stack discloses, in Fig. 4, that the start-up portion [108] includes a capacitor [C8] that collects charge prior to triggering of the inverter starting circuit (see col. 6, line 56 – col. 7, line 7).

With respect to claim 7, Stack discloses that the capacitor [C8] charges to a threshold voltage (which is of diac [D9]; see col. 6, lines 56-65).

With respect to claim 8, Stack discloses, in Fig. 4, that the start-up portion [108] includes a diac [D9] that has a breakdown voltage that determines the threshold voltage (see col. 6, lines 56-65).

With respect to claim 9, Stack discloses, in Fig. 4, that the charging capacitor [C8] charges to the breakdown voltage prior to triggering the inverter starting circuit (see col. 6, lines 56-65).

With respect to claim 11, Stack discloses, in Fig. 4, a lamp inverter starting circuit and a corresponding method of firing a lamp [FL1] comprising (1) supplying an AC line voltage (AC of 120 V or 230 V; see Fig. 4), (2) converting the AC line voltage into a DC bus voltage (via rectifier [D1, ..., D4]; see Fig. 4), (3) charging a capacitor [C8] with current supplied by the bus voltage (see col. 6, lines 56-65), (4) overcoming a breakdown voltage of a diac [D9], turning the diac [D9] conductive when the charge capacitor [C8] reaches the diac breakdown voltage (see col. 6, line 56 – col. 7, line 7), and (5) supplying voltage to the lamp [FL1] after the diac [D9] turns conductive.

With respect to claim 12, Stack discloses, in Fig. 4, that the step of overcoming the breakdown voltage includes discharging the capacitor [C8] (see col. 6, lines 56-65).

With respect to claim 13, Stack discloses, in Fig. 4, that the step of supplying the AC line voltage includes electrically connecting the lamp [FL1] to an AC voltage source, the voltage source ranging from 120 V to 230 V (which is within the claimed range of 120-280 V).

With respect to claim 16, Stack discloses, in Fig. 4, that the step of supplying voltage to the lamp [FL1] occurs before the bus voltage reaches a steady state (see col. 5, lines 24-34).

With respect to claim 17, Stack discloses, in Fig. 4, a lamp inverter starting circuit comprising (1) a switching portion [110] that includes first and second transistors [Q1, Q2], (2) a resonant load portion [T5, C9] for receiving a lamp [FL1], (3) a power factor correction circuit [106] (see col. 5, line 31) that delivers a bus voltage, and (4) a voltage dependent start-up portion [108] that delays firing (via diac [D9]; see col. 6, lines 45-67; and col. 7, lines 1-7) of the inverter until the bus voltage ramps up to a predetermined threshold (which is of the diac [D9]; see col. 6, lines 56-65).

With respect to claim 18, Stack further discloses, in Fig. 4, an AC line voltage that ranges from 120 V to 230 V (which is within the claimed range of 120-280 V).

With respect to claim 19, Stack discloses, in Fig. 4, that the bus voltage ranges from 120 V to 230 V (which is within the claimed range of 120-280 V or more).

With respect to claim 20, Stack discloses, in Fig. 4, that the voltage dependent start-up portion [108] allows firing of the inverter circuit before the bus voltage reaches a steady state (see col. 5, lines 24-34).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 10, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stack (U.S. Patent No. 6,222,322).

With respect to claim 5, Stack discloses, in Fig. 4, all of the claimed subject matter, as expressly recited in claim 1, except for specifying that the bus voltage ranges up to 390 V. However, Stack discloses the configuration of a protection circuit [112] to monitor the lamp driving current during the operation of the inverter for a prevention of damage occurrences due to overheating or excessive current flow (see col. 4, line 61 – col. 5, line 9). With this protection circuit in line, to feed in a bus voltage of up to 390 Volts to operate the lamp ballast inverter circuit of Stack with a high power-operating lamp would have been deemed obvious to a person skilled in the art.

With respect to claim 10, Stack discloses, in Fig. 4, all of the claimed subject matter, as expressly recited in claims 1 and 6-7, except for specifying that the threshold voltage is 390 V. However, Stack discloses that such a threshold voltage depends on the characteristics of the diac [D9] (see col. 6, lines 56-63). Furthermore, Stack teaches the configuration of a protection circuit [112] to monitor the lamp driving current during the operation of the inverter for a prevention of damage occurrences due to overheating or excessive current flow (see col. 4, line 61 – col. 5, line 9). With this protection circuit in line, to select a diac with high-voltage operating characteristics to define a threshold voltage of 390 V for the ballast inverter circuit of Stack to efficiently drive the inverter circuit therein would have been deemed obvious to a person skilled in the art.

With respect to claim 14, Stack discloses, in Fig. 4, all of the claimed subject matter, as expressly recited in claim 11, except for specifying that the step of overcoming the breakdown voltage includes ramping the bus voltage up to between 300V and 500V. However, Stack discloses the configuration of a protection circuit [112] to monitor the lamp driving current

during the operation of the inverter for a prevention of damage occurrences due to overheating or excessive current flow (see col. 4, line 61 – col. 5, line 9). With this protection circuit in line, to ramp up or to feed in a bus voltage of up to between 300V and 500V to operate the lamp ballast inverter circuit of Stack with a high power operating lamp would have been deemed obvious to a person skilled in the art.

With respect to claim 15, Stack discloses, in Fig. 4, all of the claimed subject matter, as expressly recited in claim 11, except for specifying that the step of overcoming the breakdown voltage includes ramping the bus voltage up to 390V. However, Stack discloses the configuration of a protection circuit [112] to monitor the lamp driving current during the operation of the inverter for a prevention of damage occurrences due to overheating or excessive current flow (see col. 4, line 61 – col. 5, line 9). With this protection circuit in line, to ramp up or to feed in a bus voltage of up to 390V to operate the lamp ballast inverter circuit of Stack with a high power operating lamp would have been deemed obvious to a person skilled in the art.

Citation of relevant prior art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Stack (U.S. Patent No. 6,781,326) discloses a lamp ballast circuit.

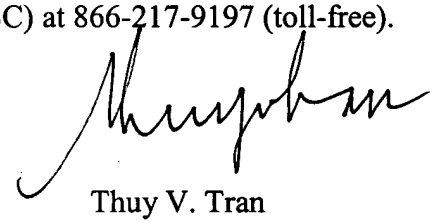
Prior art Hesterman (U.S. Patent No. 5,838,181) discloses a pulse-width modulation circuit for use in a power correction circuit.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thuy V. Tran
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Art Unit 2821

11/14/2004